In the Claims:

Claims 1-13 (Cancelled).

14. (New) A memory device comprising:

a plurality of memory modules for performing memory operations and generating power requests therefor;

a plurality of charge pump circuits for generating supply voltages for said memory modules; and

an arbitrator for receiving the power requests from said memory modules, sorting the power requests for said charge pump circuits based upon a priority scale, and distributing the supply voltages from said charge pump circuits to said memory modules based upon the sorted power requests.

15. (New) The memory device of Claim 14 wherein said arbitrator comprises:

a sorting block connected to said memory modules for sorting the power requests and generating a sorting signal based thereon; and

a switching block connected between said memory modules and said charge pump circuits for providing the sorted power requests to said charge pump circuits based upon the sorting signal, and distributing the supply voltage from said charge pump circuits to said memory modules based upon the sorted power requests.

16. (New) The memory device of Claim 15 wherein said switching block provides request allocation signals to

said sorting block, and wherein said sorting block sorts the power requests based thereon.

17. (New) The memory device of Claim 16 further comprising a plurality of request decoders connected between said charge pump circuits and said switching block, said request decoders receiving the power requests from said switching block and generating the request allocation signals therefor.

18. (New) The memory device of Claim 17 further comprising a plurality of driving circuits for said charge pump circuits connected to said request decoders in a multiplexed relationship.

19. (New) The memory device of Claim 18 wherein said driving circuits control power-down and stand-by conditions of said charge pump circuits.

20. (New) The memory device of Claim 17 wherein said request decoders generate activation signals and stand-by mode signals for respective charge pump circuits.

21. (New) The memory device of Claim 17 wherein said charge pump circuits further generate validity signals for said request decoders indicating that respective supply voltages have been reached.

22. (New) The memory device of Claim 14 wherein the priority scale is based upon at least one of request states of the power requests, priority information associated with the power requests, and positions of memory modules generating respective power requests.

23. (New) The memory device of Claim 22 wherein the request states comprise active request states and new request states.

24. (New) The memory device of Claim 14 further comprising at least one bi-directional bus connecting said arbitrator and said memory modules; wherein said memory modules further generate operation identification signals and priority signals for respective power requests; and wherein said memory modules provide the operation identification signals and priority signals to said arbitrator via said at least one bi-directional bus.

25. (New) The memory device of Claim 14 wherein said arbitrator receives a clock signal and processes the power requests within a clock cycle thereof.

26. (New) A arbitrator for distributing supply voltages from a plurality of charge pump circuits to a plurality of memory modules, the memory modules generating power requests, the arbitrator comprising:

a sorting block connected to the memory modules for sorting the power requests for the charge pump circuits based

upon a priority scale and generating a sorting signal based thereon; and

a switching block connected between the memory modules and the charge pump circuits for providing the sorted power requests to said charge pump circuits based upon the sorting signal, and distributing the supply voltage from said charge pump circuits to said memory modules based upon the sorted power requests.

27. (New) The arbitrator of Claim 26 wherein said switching block provides request allocation signals to said sorting block, and wherein said sorting block sorts the power requests based thereon.

28. (New) The arbitrator of Claim 27 further comprising a plurality of request decoders connected between the charge pump circuits and said switching block, said request decoders receiving the power requests from said switching block and generating the request allocation signals therefor.

29. (New) The arbitrator of Claim 28 further comprising a plurality of driving circuits for the charge pump circuits connected to said request decoders in a multiplexed relationship.

30. (New) The arbitrator of Claim 28 wherein said request decoders generate activation signals and stand-by mode signals for respective charge pump circuits.

31. (New) The arbitrator of Claim 26 wherein the priority scale is based upon at least one of request states of the power requests, priority information associated with the power requests, and positions of memory modules generating respective power requests.

32. (New) The arbitrator of Claim 31 wherein the request states comprise active request states and new request states.

33. (New) A method for distributing supply voltages from a plurality of charge pump circuits to a plurality of memory modules comprising:

generating power requests for the memory modules;

sorting the power requests for the charge pump circuits based upon a priority scale; and

distributing the supply voltages from the charge pump circuits to the memory modules based upon the sorted power requests.

34. (New) The method of Claim 33 wherein the priority scale is based upon at least one of request states of the power requests, priority information associated with the power requests, and positions of memory modules generating respective power requests.

35. (New) The method of Claim 34 wherein the request states comprise active request states and new request states.

36. (New) A computer-readable medium having computer-executable instructions for performing steps for distributing supply voltages from a plurality of charge pump circuits to a plurality of memory modules, the memory modules generating power requests for supply voltages, the steps comprising:

sorting the power requests for the charge pump circuits based upon a priority scale; and

distributing the supply voltages from the charge pump circuits to the memory modules based upon the sorted power requests.

37. (New) The computer-readable medium of Claim 36 wherein the priority scale is based upon at least one of request states of the power requests, priority information associated with the power requests, and positions of memory modules generating respective power requests.

38. (New) The computer-readable medium of Claim 37 wherein the request states comprise active request states and new request states.